CD54/74HC123, CD54/74HCT123, CD74HC423, CD74HCT423

Data sheet acquired from Harris Semiconductor
SCHS142A

September 1997 - Revised May 2000

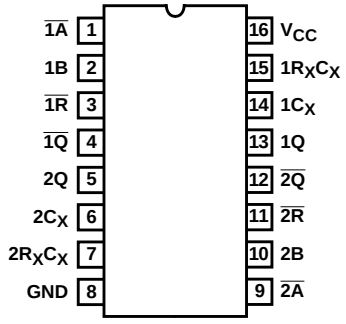
High Speed CMOS Logic Dual Retriggerable Monostable Multivibrators with Resets

Features

- **Overriding Reset Terminates Output Pulse**
- **Triggering From the Leading or Trailing Edge**
- **Q and $\overline{Q}$ Buffered Outputs**
- **Separate Resets**
- **Wide Range of Output-Pulse Widths**
- **Schmitt Trigger on Both $\overline{A}$ and B Inputs**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55^{O}C to 125^{O}C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30%of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Pinout

CD54HC123, CD54HCT123
(CERDIP)
CD74HC123, CD74HCT123, CD74HC423, CD74HCT423
(PDIP, SOIC)
TOP VIEW



Description

The ’HC123, ’HCT123, CD74HC423 and CD74HCT423 are dual monostable multivibrators with resets. They are all retriggerable and differ only in that the 123 types can be triggered by a negative to positive reset pulse; whereas the 423 types do not have this feature. An external resistor (R_X) and an external capacitor (C_X) control the timing and the accuracy for the circuit. Adjustment of Rx and C_X provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. Pulse triggering on the $\overline{A}$ and B inputs occur at a particular voltage level and is not related to the rise and fall times of the trigger pulses.

Once triggered, the output pulse width may be extended by retriggering inputs $\overline{A}$ and B. The output pulse can be terminated by a LOW level on the Reset (R) pin. Trailing edge triggering ($\overline{A}$) and leading edge triggering (B) inputs are provided for triggering from either edge of the input pulse. If either Mono is not used each input on the unused device ($\overline{A}$, B, and $\overline{R}$) must be terminated high or low.

The minimum value of external resistance, Rx is typically 5kΩ. The minimum value external capacitance, C_X, is 0pF. The calculation for the pulse width is $t_W = 0.45\ R_X C_X$ at V_{CC} = 5V.

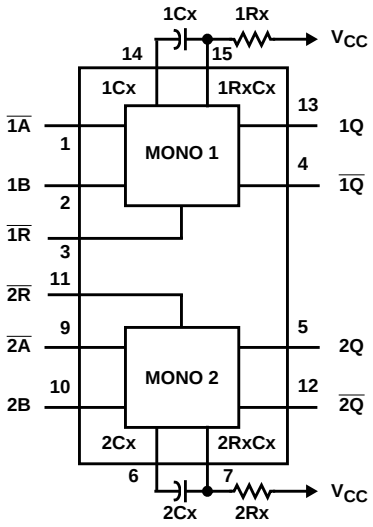
Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE
CD54HC123F	-55 to 125	16 Ld CERDIP
CD54HC123F3A	-55 to 125	16 Ld CERDIP
CD74HC123E	-55 to 125	16 Ld PDIP
CD74HC123M	-55 to 125	16 Ld SOIC
CD54HCT123F3A	-55 to 125	16 Ld CERDIP
CD74HCT123E	-55 to 125	16 Ld PDIP
CD74HCT123M	-55 to 125	16 Ld SOIC
CD74HC423E	-55 to 125	16 Ld PDIP
CD74HC423M	-55 to 125	16 Ld SOIC
CD74HCT423E	-55 to 125	16 Ld PDIP
CD74HCT423M	-55 to 125	16 Ld SOIC

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer or die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

Functional Diagram



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{A}$	B	$\overline{R}$	Q	$\overline{Q}$
CD74HC/HCT123				
H	X	H	L	H
X	L	H	L	H
L	↑	H	⎍	⎍
↓	H	H	⎍	⎍
X	X	L	L	H
L	H	↑	⎍	⎍
CD74HC/HCT423				
H	X	H	L	H
X	L	H	L	H
L	↑	H	⎍	⎍
↓	H	H	⎍	⎍
X	X	L	L	H

NOTE: H = High Voltage Level, L = Low Voltage Level,
X = Don't Care.

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} or I_{GND} . . . . . ±50mA

Operating Conditions

Temperature Range (T_A) . . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W)
PDIP Package 90
SOIC Package 115
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} and GND	0	5.5	-		±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC}	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE: For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
All	0.35

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g. 360µA max at 25°C.

Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V_{CC} (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
HC TYPES												
Minimum Input, Pulse Width	t_{WL}											
$\overline{A}$		2	100	-	-	125	-	-	150	-	-	ns
		4.5	20	-	-	25	-	-	30	-	-	ns
		6	17	-	-	21	-	-	26	-	-	ns
B	t_{WH}	2	100	-	-	125	-	-	150	-	-	ns
		4.5	20	-	-	25	-	-	30	-	-	ns
		6	17	-	-	21	-	-	26	-	-	ns

Prerequisite for Switching Specifications (Continued)

PARAMETER	SYMBOL	V_{CC} (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$\overline{R}$	t_{WL}	2	100	-	-	125	-	-	150	-	150	ns
		4.5	20	-	-	25	-	-	30	-	30	ns
		6	17	-	-	21	-	-	26	-	26	ns
$\overline{A}$ and B Hold Time	t_H	2	50	-	-	65	-	-	75	-	75	ns
		4.5	10	-	-	13	-	-	15	-	15	ns
		6	9	-	-	11	-	-	13	-	13	ns
Reset Removal Time	t_{REM}	2	50	-	-	65	-	-	75	-	75	ns
		4.5	10	-	-	13	-	-	15	-	15	ns
		6	9	-	-	11	-	-	13	-	13	ns
Retrigger Time Number	t_{rT}	5	-	-	-	-	-	-	-	-	-	ns
R_X = 10KΩ, C_X = 0			-	50	-	-	63	-	-	76	-	ns
Output Pulse Width Q or $\overline{Q}$ R_X = 10KΩ, C_X = 10nF	t_W	5	40	-	50	38.7	-	51.3	38.2	-	51.8	µs
HCT TYPES												
Minimum Input, Pulse Width $\overline{A}$	t_{WL}	5	20	-	-	25	-	-	30	-	-	- ns
B	t_{WH}		20	-	-	25	-	-	30	-	-	ns
$\overline{R}$	t_{WL}		20	-	-	25	-	-	30	-	-	ns
$\overline{A}$ and B Hold Time	t_H	5	10	-	-	13	-	-	15	-	-	ns
Reset Removal Time	t_{REM}	5	10	-	-	13	-	-	15		-	ns
Retrigger Time Number (Note 4) R_X = 10KΩ, C_X = 0	t_{rT}	5	-	50	-	-	63	-	-	76	-	ns
Output Pulse Width Q or Q R_X = 10KΩ, C_X = 10nF	t_W	5	40	-	50	38.7	-	51.3	38.2	-	51.8	µs

NOTE:

4. Time to trigger depends on the values of R_X and C_X. The output pulse width can only be extended when the time between the active-going edges of the trigger input pulses meet the minimum retrigger time requirement.

Switching Specifications C_L = 50pF, Input t_r, t_f = 6ns, R_X = 10KΩ, C_X = 0

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Trigger Propagation Delay $\overline{A}$, B, $\overline{R}$ to Q	t_{PHL}	C_L = 50pF	2	-	-	300	-	375	-	450	ns
			4.5	-	-	60	-	75	-	90	ns
		C_L = 15pF	5	-	25	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	51	-	64	-	76	ns
$\overline{A}$, B, $\overline{R}$ to $\overline{Q}$	t_{PHL}	C_L = 50pF	2	-	-	320	-	400	-	480	ns
			4.5	-	-	64	-	80	-	96	ns
		C_L = 15pF	5	-	26	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	54	-	68	-	82	ns
Reset Propagation Delay $\overline{R}$ to Q or $\overline{Q}$	t_{PHL}, t_{PLH}	C_L = 50pF	2	-	-	215	-	270	-	325	ns
			4.5	-	-	43	-	54	-	65	ns
			6	-	-	37	-	46	-	55	ns
Output Transition Time	t_{THL}, t_{TLH}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Output Pulse Width R_X = 10KΩ, C_X = 10pF	-	-	5	-	45	-	-	-	-	-	µs
Pulse Width Match Between Circuits In the Same Package R_X = 10KΩ, C_X = 10pF	-	-	5	-	±2	-	-	-	-	-	%
Power Dissipation Capacitance (Notes 5, 6)	C_{PD}	C_L = 15pF	5	-	-	-	-	-	-	-	pF
Input Capacitance	C_{IN}	C_L = 50pF	-	10	-	10	-	10	-	10	pF

NOTES:

5. C_{PD} is used to determine the dynamic power consumption, per multivibrator.
6. $P_D = (C_{PD} + C_X) V_{CC}^2 f_i \Sigma(C_L V_{CC}^2 f_O)$ where f_i = input frequency, f_O = Output Frequency, C_L = Output Load Capacitance, C_X = External Capacitance V_{CC} = Supply Voltage assuming $f_i \ll \frac{1}{t_W}$

Test Circuits and Waveforms

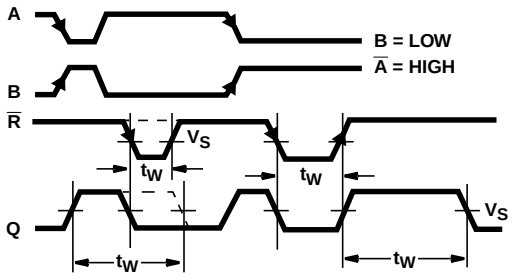


FIGURE 1. OUTPUT PULSE CONTROL USING RESET INPUT ($\overline{R}$) PULSE FOR 123

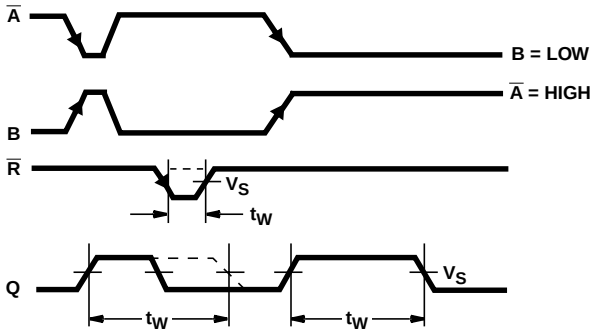
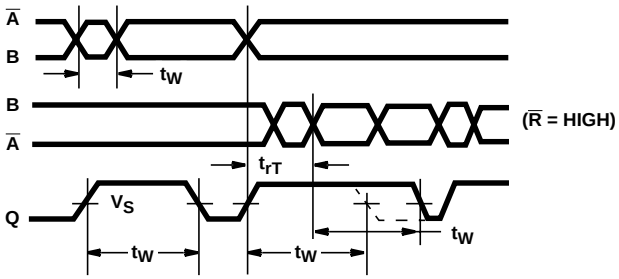


FIGURE 2. OUTPUT PULSE CONTROL USING RESET INPUT ($\overline{R}$) FOR 423



NOTE: Output pulse control using retrigger pulse for 123 and 423.

FIGURE 3. TRIGGERING OF ONE SHOT BY INPUT $\overline{A}$ OR INPUT B FOR A PERIOD t_W

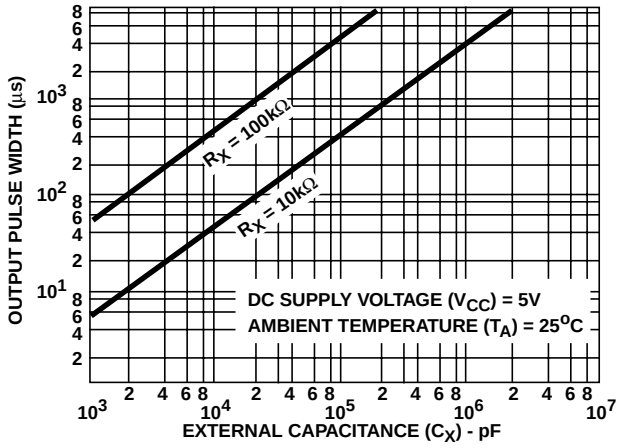


FIGURE 4. TYPICAL OUTPUT PULSE WIDTH AS A FUNCTION OF C_X FOR R_X = 10kΩ AND 100kΩ

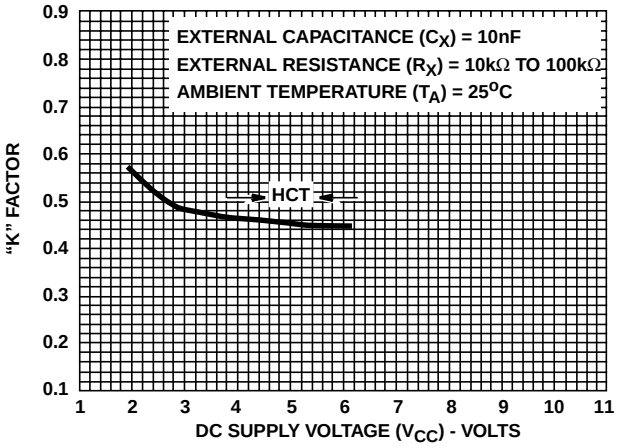


FIGURE 5. TYPICAL "K" FACTOR AS A FUNCTION OF V_{CC}

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